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de Heer

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(54) **GRAPHENE TRANSISTOR**

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USPC 257/288, 368, 369; 438/151, 197, 199; 977/734, 742
See application file for complete search history.

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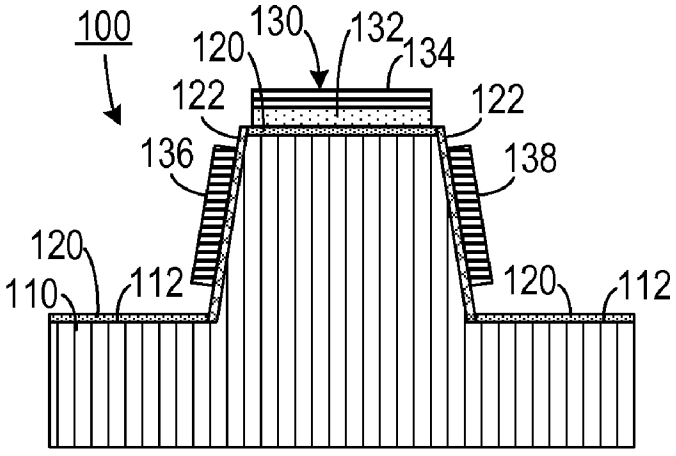
(57) **ABSTRACT**

A transistor includes a silicon carbide crystal (**110**) having a silicon terminated face (**112**). A semiconducting-type graphene layer (**120**) is bonded to the silicon terminated face (**112**). A first semimetallic-type graphene layer (**122**) is contiguous with a first portion of the semiconducting-type graphene layer (**120**). A second semimetallic-type graphene layer (**122**) is contiguous with a second portion of the semiconducting-type graphene layer (**120**) that is spaced apart from the first portion. An insulator layer (**132**) is disposed on a portion of the semiconducting-type graphene layer (**120**). A gate conductive layer (**134**) disposed on the insulator layer (**132**) and spaced apart from the semiconducting-type graphene layer (**120**).

20 Claims, 2 Drawing Sheets



(51) **Int. Cl.**

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H01L 29/06	(2006.01)
H01L 21/02	(2006.01)
H01L 29/165	(2006.01)
H01L 29/417	(2006.01)
H01L 29/78	(2006.01)

(52) **U.S. Cl.**

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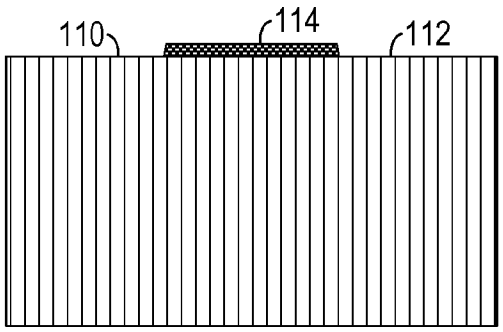

FIG. 1A

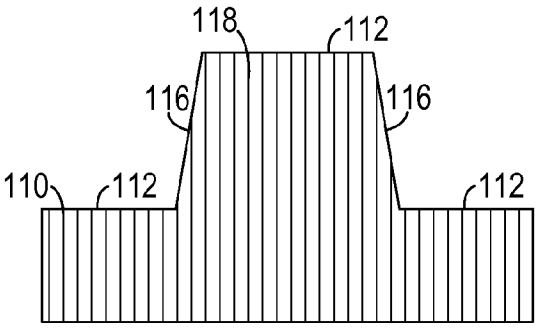

FIG. 1B

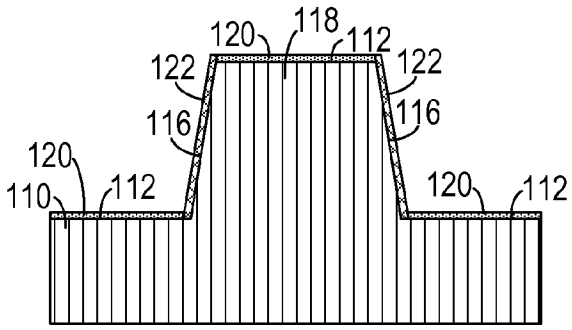

FIG. 1C

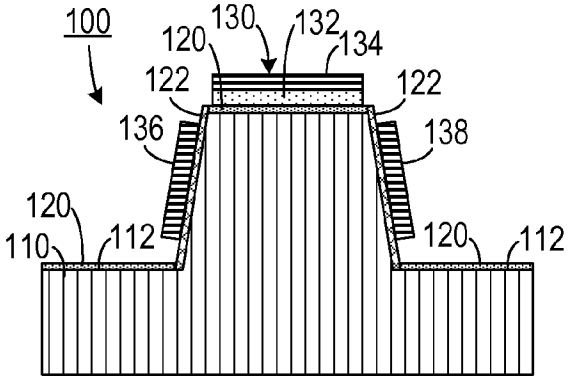

FIG. 1D

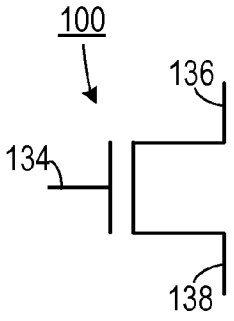

FIG. 1E

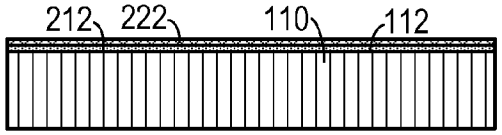

FIG. 2A

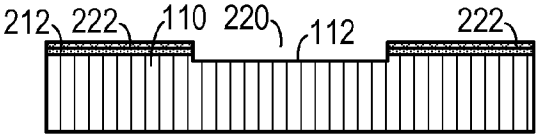

FIG. 2B

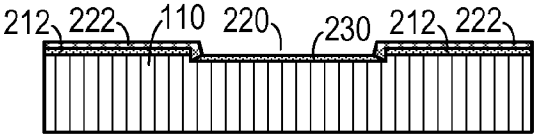

FIG. 2C

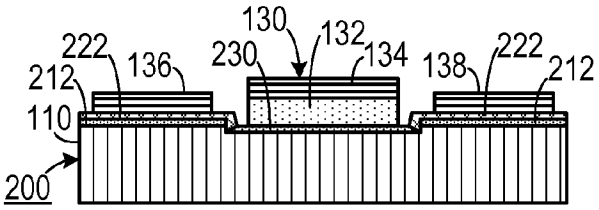

FIG. 2D

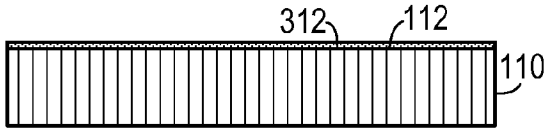

FIG. 3A

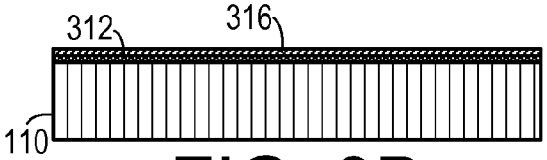

FIG. 3B

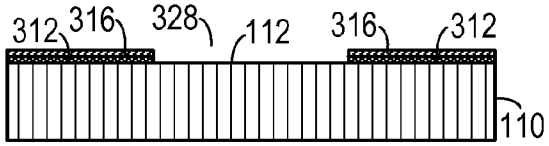

FIG. 3C

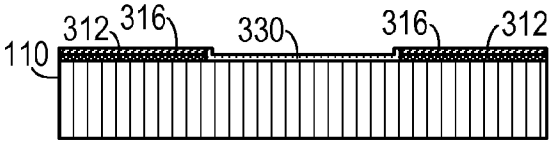

FIG. 3D

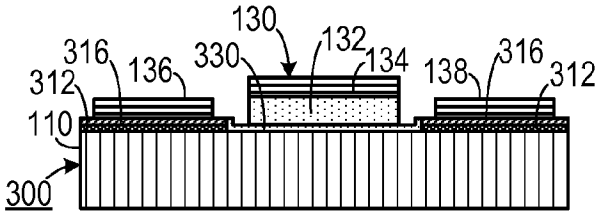

FIG. 3E

GRAPHENE TRANSISTOR

CROSS-REFERENCE TO RELATED APPLICATION(S)

This application claims the benefit of U.S. Provisional Patent Application Ser. No. 61/539,664, filed Sep. 27, 2011, the entirety of which is hereby incorporated herein by reference.

This application claims the benefit of International Patent Application No. PCT/US12/57249, filed Sep. 26, 2012, the entirety of which is hereby incorporated herein by reference.

STATEMENT OF GOVERNMENT INTEREST

This invention was made with government support under agreement No. DMR-082382, awarded by the National Science Foundation. The government has certain rights in the invention.

BACKGROUND OF THE INVENTION

1. Field of the Invention

The present invention relates to graphitic devices and, more specifically, to a graphene transistor.

2. Description of the Related Art

Microelectronic circuits are fundamental to virtually all digital systems in existence. Current circuit technology employs semiconductor transistors that are coupled to each other with conductors, such as metal and polysilicon. Electrical current flowing through such conductors results in heat generation. A circuit density increases, heat generation becomes an increasingly significant problem.

One area currently being explored involves nano-scale carbon-based circuitry. For example, carbon nanotubes have the property of ballistic charge transport, in which when current flows through a nanotube almost no heat is generated. Unfortunately, because carbon nanotubes cannot currently be grown in a pattern corresponding to a desired practical scale circuit, use of carbon nanotube circuits are not currently seen as a viable solution.

Recently, graphene circuits have been proposed. Graphene is an allotrope of carbon that is only one atom thick. Graphene circuits employ a substantially flat graphene layer that has been patterned using conventional micro-electronic lithographic patterning techniques. The graphene can be patterned into channels with dimensions approximating the dimensions of carbon nanotubes, thereby achieving near-ballistic charge transport properties.

One difficulty currently experienced with graphene based electronics is that graphene behaves as a semimetal and not a semiconductor. As a result, most graphene transistors do not effectively function as switches due to large source to drain leakage currents. As a result, most attempts at making graphene transistors result in transistors that cannot be switched off. This problem has been approached by several different methods. In one method, very narrow graphene ribbons are produced which are often observed to have a band gap. In another method, attempts have been made to chemically functionalize graphene to give the functionalized regions of the graphene semiconductor properties. These approaches have not yet yielded graphene transistors that can be used in practical applications.

Therefore, there is a need for graphene-based transistors in which regions of the graphene have semiconducting properties. There is also a need for a method of making semiconducting graphene.

SUMMARY OF THE INVENTION

The disadvantages of the prior art are overcome by the present invention which, in one aspect, is a transistor that includes a silicon carbide crystal having a silicon terminated face. A semiconducting-type graphene layer is bonded to the silicon terminated face. A first semimetallic-type graphene layer is contiguous with a first portion of the semiconducting-type graphene layer. A second semimetallic-type graphene layer is contiguous with a second portion of the semiconducting-type graphene layer that is spaced apart from the first portion. An insulator layer is disposed on a portion of the semiconducting-type graphene layer. A gate conductive layer disposed on the insulator layer and spaced apart from the semiconducting-type graphene layer.

In another aspect, the invention is a method of making a transistor in which a semiconducting-type graphene layer is formed on a silicon terminated face of a silicon carbide crystal. At least one semimetallic-type graphene layer is formed adjacent to the silicon carbide crystal so that the semimetallic-type graphene layer is contiguous with the semiconducting-type graphene layer. An insulator layer is applied on a portion of the semiconducting layer. A conductor layer is applied to the insulator layer.

These and other aspects of the invention will become apparent from the following description of the preferred embodiments taken in conjunction with the following drawings. As would be obvious to one skilled in the art, many variations and modifications of the invention may be effected without departing from the spirit and scope of the novel concepts of the disclosure.

BRIEF DESCRIPTION OF THE FIGURES OF THE DRAWINGS

FIGS. **1**A-**1**E are a schematic diagrams demonstrating a sidewall embodiment.

FIGS. **2**A-**2**D are schematic diagrams demonstrating a flat embodiment.

FIGS. **3**A-**3**E are schematic diagrams demonstrating a passivated layer embodiment.

DETAILED DESCRIPTION OF THE INVENTION

A preferred embodiment of the invention is now described in detail. Referring to the drawings, like numbers indicate like parts throughout the views. Unless otherwise specifically indicated in the disclosure that follows, the drawings are not necessarily drawn to scale. As used in the description herein and throughout the claims, the following terms take the meanings explicitly associated herein, unless the context clearly dictates otherwise: the meaning of "a," "an," and "the" includes plural reference, the meaning of "in" includes "in" and "on."

Methods of making thin film graphene on silicon carbide crystals through annealing are shown in U.S. Pat. No. 7,015,142, and in U.S. Patent Publication No. US-2009-0226638-A1, both of which are incorporated herein by reference.

As shown in FIGS. **1**A-**1**E, one embodiment of a transistor **100** is formed on a silicon terminated face **112** (e.g., the 0001 face) of a silicon carbide crystal **110**. A mask **114** may be applied to the silicon terminated face **112**, which is then subject to an etching process (e.g., oxygen plasma etching, chemical etching, ion beam etching, etc.) so as to form a raised portion **118** having opposing sidewalls **116**. Because the sidewalls **116** are transverse to the silicon terminated face, they are not silicon terminated. As shown in FIG. **1**C, the

resulting crystal **110** is subjected to an annealing process (e.g., by heating it to a temperature of between 1000° C. and 2000° C. in a partial vacuum) that causes silicon atoms to evaporate from the crystal **110**, leaving a layer 0-type graphene layer **120** (referred to as a "buffer layer") on the silicon terminated face **112** and a layer of 1-type graphene layer **122** on the sidewalls **116**. The layer 0-type graphene layer **120** is contiguous with the layer 1-type graphene layer **122** and the junction between the two layers is seamless. Because the layer 0-type graphene layer **120** is bonded directly to the silicon terminated face **112** of the crystal **110**, it exhibits the properties of a semiconductor such that it exhibits a band gap of about 0.3 eV-0.5 EV. Because the layer 1-type graphene layer **122** on the sidewalls **116** is not bonded to a silicon terminated face, it exhibits semimetallic properties and can act as a conductor. The top-most layers of graphene (whether layer 0-type or layer 1-type) will be contiguous and join seamlessly.

As shown in FIG. **1**D, a dielectric insulator layer **132** is deposited on a top portion of the layer 0-type graphene layer **120** and a first conductor layer (e.g., a metal layer) **134** is deposited on the dielectric insulator layer **132**. Together, these two layers form a gate **130**. A second conductor layer **136** is deposited on one of the layer 1-type graphene layers **122** to form a source contact and a third conductor layer **138** is deposited on one of the layer 1-type graphene layers **122** to form a drain contact. This structure can be modeled as a transistor **100**, as shown in FIG. **1**E.

In another embodiment, as shown in FIGS. **2**A-**2**D, at least two graphene layers are grown on the silicon terminated face **112** of a silicon carbide crystal **110** through a first annealing process in which silicon atoms are evaporated from the surface of the crystal **110**. The graphene layers include a layer 0-type layer **212** that is bonded to the silicon terminated face **112** and at least one layer 1-type layer **222** that is bonded to the layer 0-type layer **212**. As shown in FIG. **2**B, an area **220** is etched into the two layers, thereby exposing a portion of the silicon terminated face **112** of the silicon carbide crystal **110**. (In one example, an oxygen plasma etch is employed.) As shown in FIG. **2**C, a second layer 0-type graphene layer **230** is then grown on the exposed portion of the silicon terminated face **112** through a second annealing process. This layer 0-type graphene layer **230** acts as a semiconductor, whereas the remaining layer 1-type graphene layers **222** have semimetallic conducting properties. A gate structure **130**, as described above, is deposited on to the second layer 0-type graphene layer **230** and a source contact **136** and a drain contact **138** are deposited on to the layer 1-type graphene layers **222**, as shown in FIG. **2**D.

In yet another embodiment, as shown in FIGS. **3**A-**3**E, a graphene buffer layer **312** is grown on a silicon terminated face **112** of a silicon carbide crystal **110**. As shown in FIG. **3**B, the surface **112** of the silicon carbide crystal **110** is passivated by subjecting it to a hydrogen gas environment, thereby forming a passivated silicon carbide surface **112**. As a result, the bonds between the silicon carbide crystal **110** and the graphene layer **312** are broken and the graphene layer is now a layer 0*-type layer (which may be referred to as "passivated graphene"), which is quasi free standing and which acts as a semimetallic layer. In one experimental example, the hydrogen-rich environment included a one atmosphere partial pressure of hydrogen and the graphene layer **312** was heated to about 550° C. for about 75 minutes in the hydrogen-rich environment. As shown in FIG. **3**C, an opening **328** is etched to expose a portion of the silicon terminated face **112**. As shown in FIG. **3**D, a second annealing results in a second layer 0-type graphene layer forming on the exposed portion of the silicon terminated face **112**, which couples seamlessly to the layer 0*-type graphene layer **316**. A gate structure **130**, as described above, is deposited on to the layer 0-type graphene layer **330** and a source contact **136** and a drain contact **138** are deposited on to the layer 0*-type graphene layers **316**, as shown in FIG. **3**E. A portion of the layer 0*-type graphene layer **316** can be converted back to layer 0-type graphene by subjecting it to a hydrogen-poor environment (e.g., a partial vacuum) and heating it (e.g., to about 900° C.) for a predetermined amount of time.

The above embodiments may employ one of many known patterning processes to generate complex integrated circuits. When the sources and drains of the above disclosed transistors are subjected to a suitable bias voltage and when the gates are subjected to a gate voltage, the resulting field generated by the gate will cause current to flow through the semiconducting layer 0-type graphene subjected to the field. Thus, these transistors act as switches, thereby making them suitable for digital circuit applications.

The above described embodiments, while including the preferred embodiment and the best mode of the invention known to the inventor at the time of filing, are given as illustrative examples only. It will be readily appreciated that many deviations may be made from the specific embodiments disclosed in this specification without departing from the spirit and scope of the invention. Accordingly, the scope of the invention is to be determined by the claims below rather than being limited to the specifically described embodiments above.

What is claimed is:

1. A transistor, comprising:

(a) a silicon carbide crystal having a silicon terminated face;

(b) a semiconducting-type graphene layer bonded to the silicon terminated face;

(c) a first semimetallic-type graphene layer contiguous with a first portion of the semiconducting-type graphene layer;

(d) a second semimetallic-type graphene layer contiguous with a second portion of the semiconducting-type graphene layer that is spaced apart from the first portion;

(e) an insulator layer disposed on a portion of the semiconducting-type graphene layer; and

(f) a gate conductive layer disposed on the insulator layer and spaced apart from the semiconducting-type graphene layer.

2. The transistor of claim **1**, wherein the semiconducting-type graphene layer comprises a layer 0-type graphene.

3. The transistor of claim **1**, wherein at least one of the first semimetallic-type graphene layer and the second semimetallic-type graphene layer comprises a layer 1-type graphene.

4. The transistor of claim **1**, wherein at least one of the first semimetallic-type graphene layer and the second semimetallic-type graphene layer is formed adjacent to a non-silicon terminated face of the silicon carbide crystal.

5. The transistor of claim **4**, wherein the silicon terminated face comprises a horizontal surface of the silicon carbide crystal and wherein the non-silicon terminated face comprises a sidewall of the silicon carbide crystal.

6. The transistor of claim **1**, wherein at least one of the first semimetallic-type graphene layer and the second semimetallic-type graphene layer is formed on a layer 0-type graphene layer.

7. The transistor of claim **1**, wherein at least one of the first semimetallic-type graphene layer and the second semimetallic-type graphene layer comprises passivated graphene.

8. The transistor of claim 7, wherein passivated graphene is formed on passivated silicon carbide.

9. The transistor of claim 1, wherein the gate conductive layer comprises a metal.

10. The transistor of claim 1, further comprising:

(a) a metal source contact affixed to the first semimetallic-type graphene layer; and

(b) a metal drain contact affixed to the second semimetallic-type graphene layer.

11. A method of making a transistor, comprising the steps of:

(a) forming a semiconducting-type graphene layer on a silicon terminated face of a silicon carbide crystal;

(b) forming at least one semimetallic-type graphene layer adjacent to the silicon carbide crystal so that the semimetallic-type graphene layer is contiguous with the semiconducting-type graphene layer;

(c) applying an insulator layer on a portion of the semiconducting layer; and

(d) applying a conductor layer to the insulator layer.

12. The method of claim 11, wherein the step of forming a semiconducting-type graphene layer comprises evaporating silicon from the silicon carbide crystal.

13. The method of claim 11, further comprising the step of forming a raised portion on the silicon carbide crystal so that the raised portion has a silicon terminated face and at least one sidewall extending transversely therefrom so that the sidewall is not silicon terminated, wherein the semimetallic-type graphene is disposed on the sidewall.

14. The method of claim 11, wherein the step of forming at least one semimetallic-type graphene layer comprises forming a plurality of graphene layers on the silicon carbide crystal and wherein the step of forming a semiconducting-type graphene layer comprises removing a region of the plurality of graphene layers so as to expose an exposed silicon terminated face portion and then forming the semiconducting-type graphene layer on the exposed silicon terminated face portion.

15. The method of claim 11, wherein the step of forming a semimetallic-type graphene layer comprises the steps of:

(a) evaporating silicon from a selected surface of the silicon carbide crystal thereby forming a graphene layer; and

(b) passivating a portion of the selected surface of the silicon carbide crystal, thereby breaking chemical bonds between the portion of the selected surface and the silicon carbide crystal so that the selected surface becomes semimetallic-type graphene.

16. The method of claim 15, further comprising the step of forming a raised portion on the silicon carbide crystal so that the raised portion has a silicon terminated face and at least one sidewall extending transversely therefrom so that the sidewall is not silicon terminated.

17. The method of claim 15, wherein the step of passivating a portion of the selected surface of the silicon carbide crystal comprises the step of subjecting the selected surface to a hydrogen-rich environment at a preselected selected temperature for a preselected amount of time.

18. The method of claim 17, wherein the hydrogen-rich environment includes a one atmosphere partial pressure of hydrogen.

19. The method of claim 17, wherein the preselected temperature is about 550° C. and wherein the preselected amount of time is about 75 minutes.

20. The method of claim 17, further comprising the step of heating a selected portion of the semimetallic-type graphene in a hydrogen-poor environment at a temperature and for an amount of time sufficient to cause hydrogen to be removed from the selected portion, thereby causing the selected portion to become semiconducting.

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